Abstract of the Disclosure

Integrated memory circuits, key components in thousands of electronic and computer products, have recently been made using ferroelectric memory transistors, which offer faster write cycles and lower power requirements than over conventional floating-gate transistors. One problem that hinders the continued down-scaling of conventional ferroelectric memory transistors is the vulnerability of their gate insulations to failure at thinner dimensions. Accordingly, the inventors devised unique ferroelectric gate structures, one of which includes a high-integrity silicon-oxide insulative layer, a doped titanium-oxide layer, a weak-ferroelectric layer, and a control gate. The doped titanium-oxide layer replaces a metal layer in the conventional ferroelectric gate structure, and the weak-ferroelectric layer replaces a conventional ferroelectric layer. These replacements reduce the permittivity mismatch found in conventional gate structures, and thus reduce stress on gate insulation layers, thereby improving reliability of ferroelectric memory transistors, particularly those with thinner gate insulation.